

MCS7840

Printed Circuit Board Design (PCB) Guidelines

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Revision History

Name	Date	Reason For rewrite	Version
K.Srinivas	06 th April2007	Initial Draft	1.0

1.Introduction :

System operation frequencies are increasing, PCB layout is becoming increasingly complex. A successful high-speed PCB must effectively integrate the IC's and other components into a single design. MCS7840 has USB2.0 interface and utilize fast I/O pins. As Fast edge rates can contribute to noise generation, signal reflection, cross-talk and ground bounce; designers must be careful to handle these issues during PCB layout.

This document provides guidelines for designing MCS7840 PCB's. The Following, component placement, layout guidelines for USB are effective in designing a robust system with the MCS7840.

2.PCB Overview :

2.1 PCB Details

Figure 1a is the Top side of the MCS7840 Eval Board. Most of the components are placed on the Top side of the PCB. The decoupling capacitors are only placed on the Bottom side of the PCB.

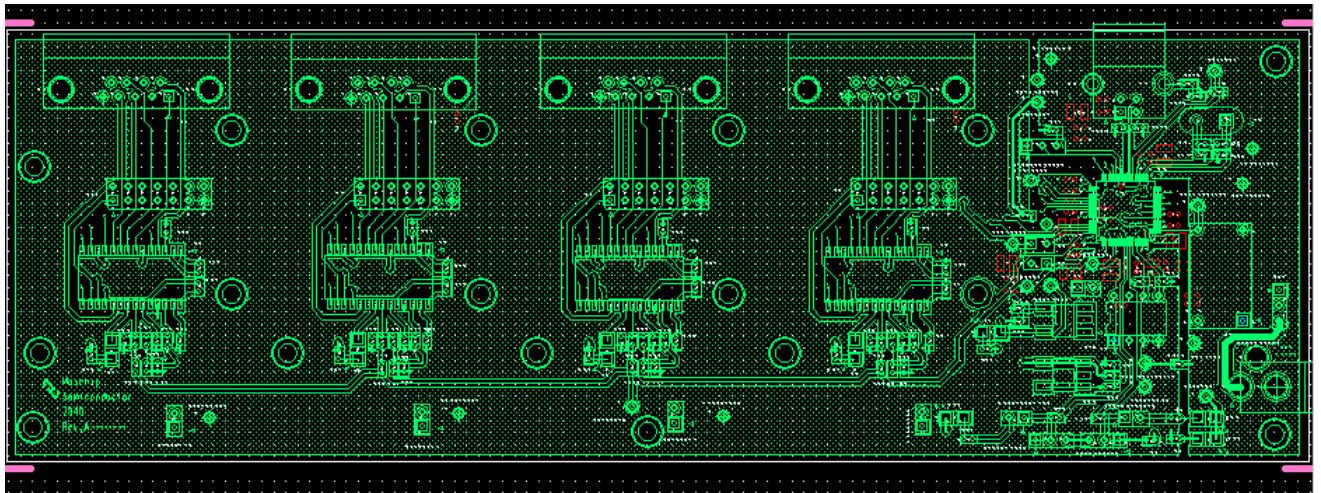


Figure 1a Top Side View

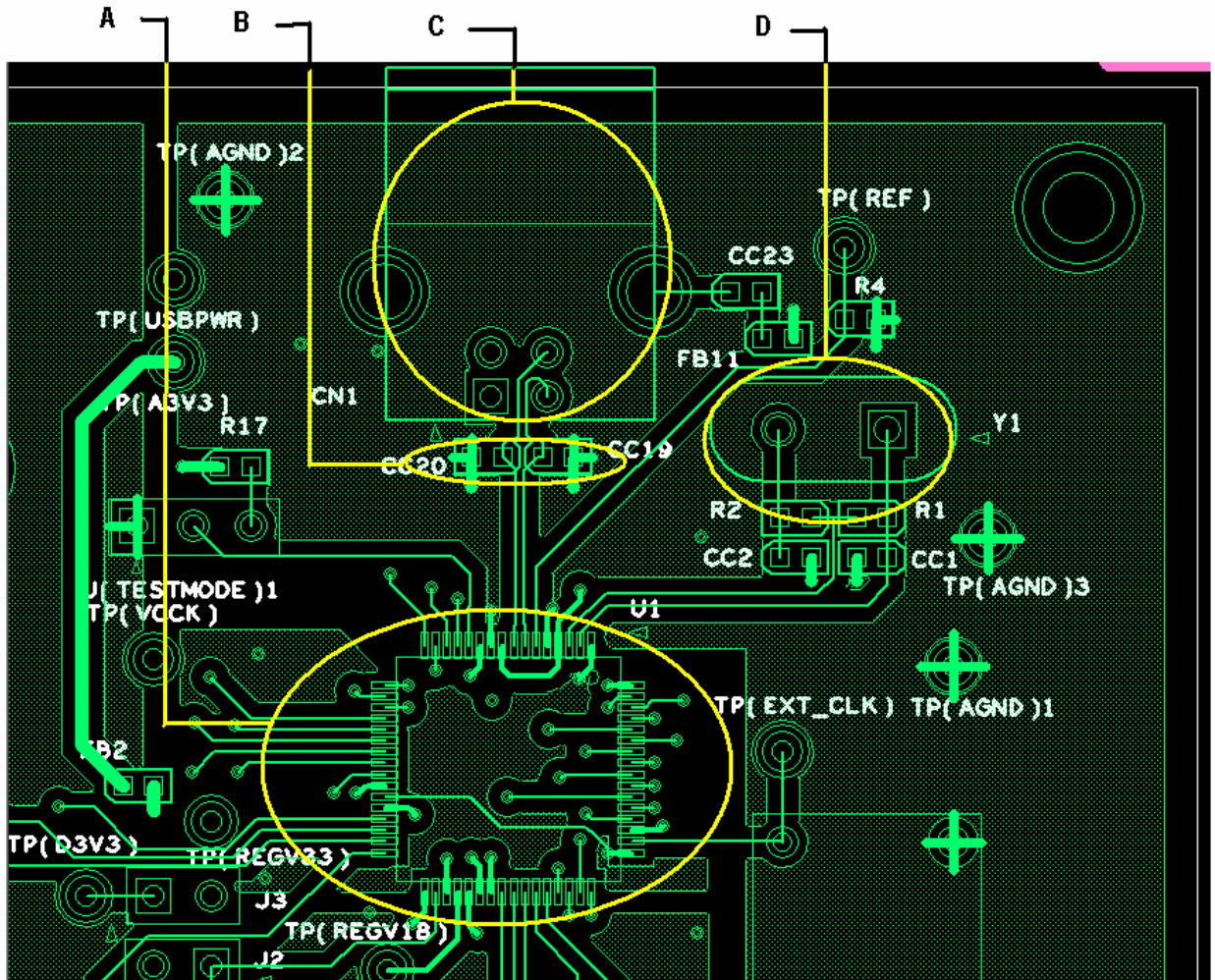


Figure 1b Top Side View (Component Placement)

2.2 Components Placement:

- A. MCS7840 CHIP.
- B. CC19 & CC20 SLEW RATE CONTROL CAPACITORS.
- C. USB type B connector.
- D. 12MHz CRYSTAL.

3. Layout Guidelines :

This layout guide discusses the important issues and provide for successful, effective board designs using MCS7840.

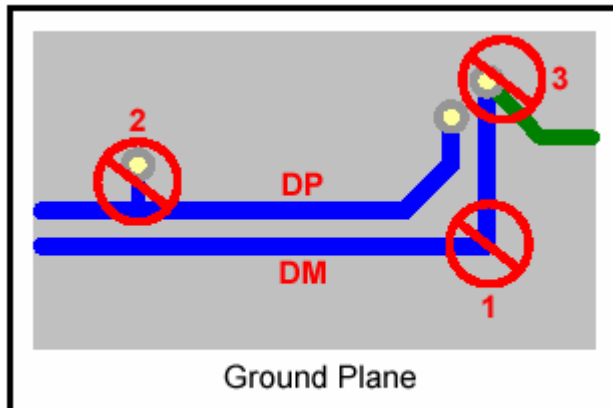
- DP and DM signals on USB2.0 differential lines
- Placement and differential signal routing
- Power delivery and power / ground distribution.

For more details please refer to the USB2.0 Specification.

3.1 USB Layout Guidelines:

3.1.1 USB Placement and Routing Guidelines:

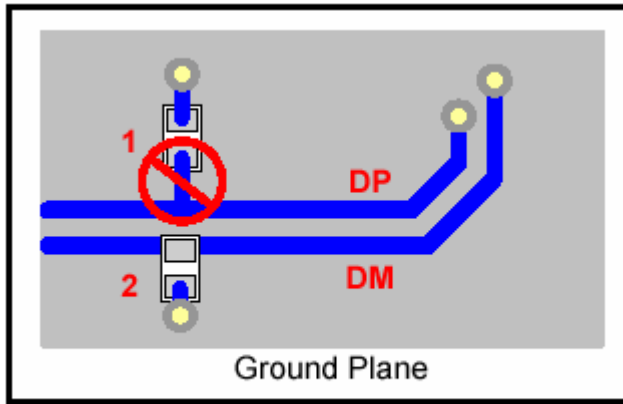
1. Place the USB type-B connector and Slew-rate control capacitors CC19 & CC20 as close as to the connector on the board as shown in Figure 1b.
2. Keep parallelism between DP and DM with the trace spacing, which achieves 90 Ohms differential impedance.
3. Route the High Speed signals like Clock and DP & DM USB signals as equal as possible with minimum trace length. Keep the maximum route spacing between USB signals and other signals.
4. Route the USB Differential signals DP & DM, on the Top side of the PCB, which is adjacent to the ground plane layer.
5. When it becomes necessary to turn 90°, use to 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.



Avoid signal reflection

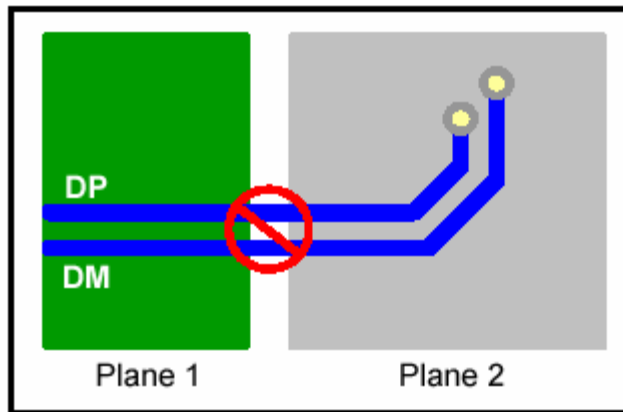
6. Do not route USB traces under crystal oscillator, clock-synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
7. Vias on differential signal traces and routing these signals too close to crossing the split ground plane will adversely affect the differential trace impedance.

8. Stubs on differential signal pair should be avoided. When stubs exist, it will cause signal reflection and affect signal quality. If a stub is unavoidable in the design, no stub should be greater than 200mils.



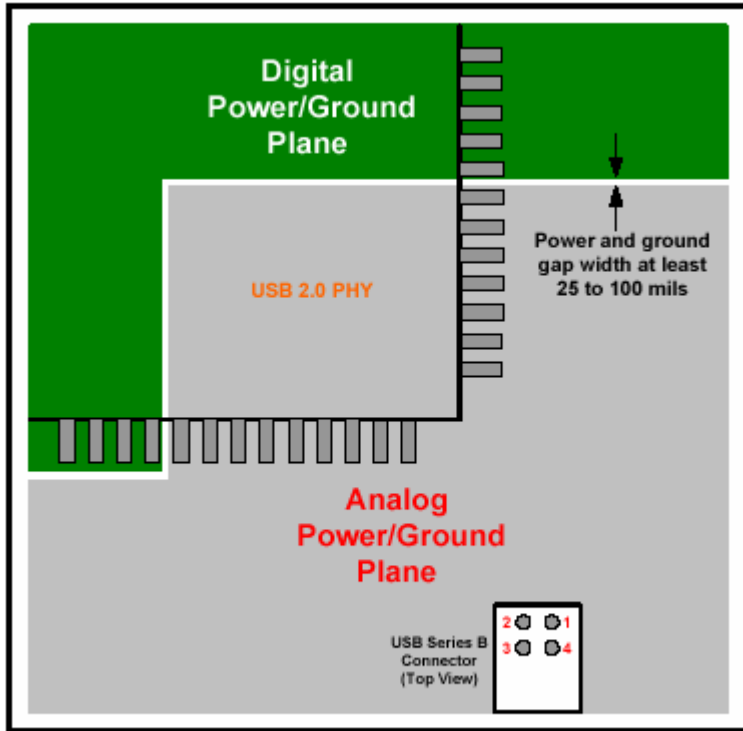
Avoid stubs on differential pair trace

9. Route differential signal pair traces over continuous ground or power planes. Avoid crossing anti-etch areas or any break in the underlying planes.



Avoid routing to break image plane (anti-etch areas)

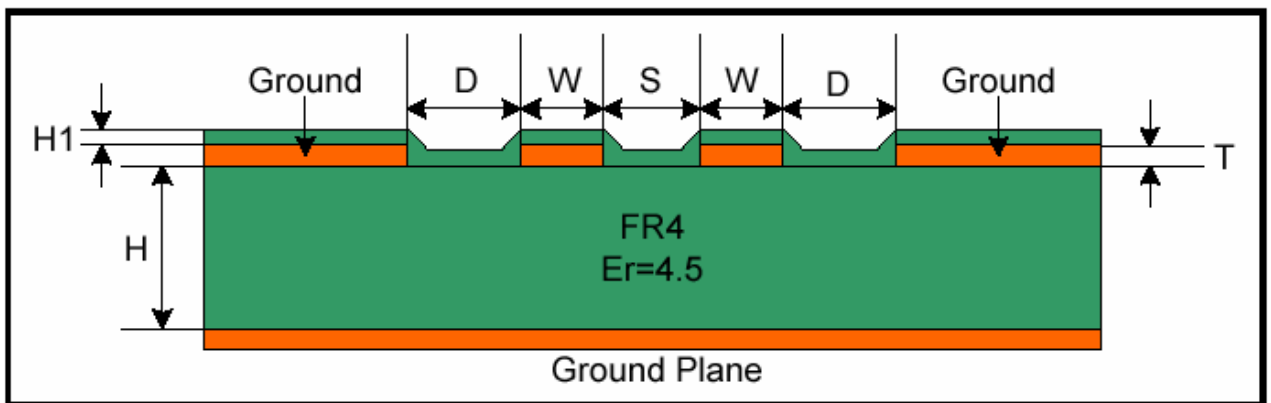
10. Provide ample power and ground planes. Avoid routing the differential signal pair near the edge of the PCB or power planes.



Power distribution

3.1.2 Trace Spacing for USB2.0.

The physical construction of differential PCB traces as shown in Figure 2, determines the differential impedance. The primary physical characteristics are summarized as follows.



Stackup digram

Figure 2

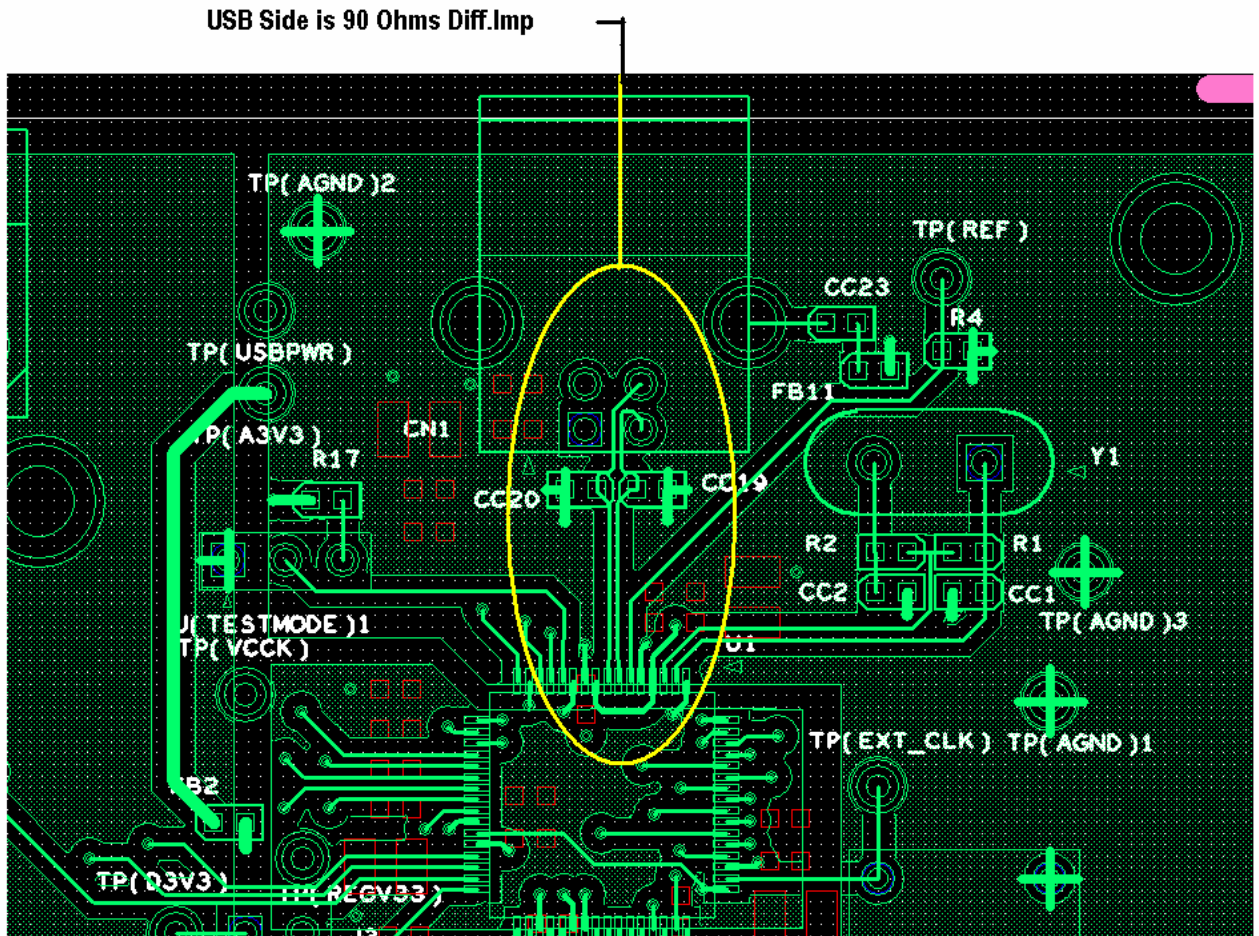
1. W = Width of the trace (7MILS)
2. S = Separation from DP (+) to DM (-) (7MILS)
3. H = Dielectric thickness, distance of trace from the ground plane is 4.5MILS (Prepeg).
4. T = Thickness of the trace (1 Ounce of Cu)
5. D = 2S In order to avoid crosstalk.
6. H1= Solder Mask Thickness.
7. Er = Dielectric constant (FR4 Er = 4.5)
8. Board Thickness=1.6mm (63mils)

3.1.3 Layer Stack up Details:

1. Top Layer.
2. GND Layer.
3. L3 Signal Layer
4. L4 Signal Layer
5. VCC Layer
6. BOTTOM Layer.

We require 90 ohms differential impedance on the USB side (DP, DM). Rest all the traces are required to have 50 ohm controlled impedance on the Board.

3.1.4 Impedance control at Fabrication Level.



3.2 Crystal Layout Guidelines:

MCS7840 uses 12MHz. Place the crystals nearer to the MCS7840 Chip and keep the clock traces as short as possible. Route the clock signals over continuous ground and power planes. Shielding or GND Plane should be provided for these clock Signals on layers.

3.3. Summary Key Points

1. Route high-speed signals over continuous ground and power planes.
2. Provide ample power and ground planes
3. Avoid stubs on the USB High Speed Signals.
4. Avoid Signal reflection on the USB High Speed Signals.
5. Ensure the power supply is rated for the load
6. Shielding is provided for USB signals, CLK signals and Oscillators' etc.

For Additional information:

Contact sales@moschip.com for commercial details. techsupport@moschip.com can be contacted for technical details.

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